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4,608,691
5,329,533

L30: Entry 24 of 25 File: USPT Nov 1, 1988

DOCUMENT-IDENTIFIER: US 4782487 A
TITLE: Memory test method and apparatus

Detailed Description Text (10):
Linear feedback shift register ("LFSR") 42 shown in FIG. 1 generates a pseudo-random sequence of data words to be written into the memory. The pseudo-random data sequence simulates the randomness of real memory use and may stimulate failure modes not discovered by more regular sequences. LFSR 42 provides a pseudo-random data sequence for generating a pattern of data. Control 14 controls the enablement and disablement of LFSR 42. The data output of LFSR 42 is input into register 22 of data path 18. After a data word generated by LFSR 42 is stored in register 22, check bits for the data word are then generated by ECC 24 and those check bits are stored in register 28. The data word in register 22 is then inputted into register 20. The data word stored in register 20 along with the check bits stored in register 28 are then input into DRAMS 16.

Detailed Description Text (15):
FIG. 5 illustrates the sequence for a memory test and FIG. 1 illustrates the apparatus employed. At step 180, a first pattern of data is written into DRAMs 16 in accordance with a pseudo-random address sequence determined by LFSR 40. For each address generated by LFSR 40, data LFSR 42 generates a pseudo-random data word, which is stored in register 22. ECC circuitry 24 generates a set of check bits for the data word, and the check bits are stored in register 28. The data word is moved to and stored in register 20, and then both the data word in register 20 (generated by LFSR 42) and its check bits in register 28 are written into DRAMs 16. Address LFSR 40 then changes to another pseudo-random address, and data LFSR changes to another pseudo-random data word, and the process of writing the data word and its check bits into DRAMs 16 is likewise repeated. FIG. 6 illustrates a portion of the pseudo-random address sequences generated by LFSR 40 and a portion of the pseudo-random data words generated by LFSR 42.

Detailed Description Text (17):
At step 184, each data word and its check bits are in turn read from DRAMs 16 according to a pseudo-random address sequence determined by LFSR 40. The data word read from DRAMs 16 is stored in register 28. At step 188, the data word and its check bits are checked for any error. ECC circuitry 24 provides a syndrome for the data word and check bits read from the DRAMs 16. Decode circuitry 30 then decodes the syndrome produced by ECC circuitry 24. If the syndrome decoded by decode 30 indicates the presence and location of a correctable error in the data, then corrector 26 corrects the bit of the data that is in error.

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L30: Entry 22 of 25 File: USPT Oct 8, 1991

DOCUMENT-IDENTIFIER: US 5056089 A
**** See image for Certificate of Correction ****
TITLE: Memory device

Detailed Description Text (7):
In the case of an E.sup.2 PROM having a page-mode writing function, the ECC code register 60 may be constituted by, for example, a linear feedback shift register (LFSR). In such an arrangement, the ECC code 30e generated by the ECC code generating circuit 30 on the basis of a plurality of write data 20d is converted into compressed data in accordance with a control clock supplied from a microprocessor, and is then stored in the LFSR. After all of a plurality of test patterns have been input, the contents of the LSFR are read out and compared with an expected value, so that it is possible to immediately check a single function of the ECC code generating circuit 30.

CLAIMS:

4. The memory system according to claim 2 wherein said register is a linear feedback shift register (LFSR) for controlling said memory device to sequentially input a plurality of test patterns to said ECC code generating circuit, to compress the ECC code output from said ECC code generating circuit in accordance with the test patterns, and to check said ECC code generating circuit on the basis of the result.

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L5: Entry 1 of 4 File: USPT Apr 10, 2001

DOCUMENT-IDENTIFIER: US 6216246 B1
TITLE: Methods to make DRAM fully compatible with SRAM using error correction code (ECC) mechanism

Detailed Description Text (26):
FIG. 2(a) is a high level block diagram describing the geometric relationship between an ECC logic circuit of the present invention and DRAM memory cells. Memory cells are represented symbolically by circles (301) in FIG. 2(a). FIG. 2(b) is a schematic diagram of a DRAM memory cell. Each memory cell (301) contains one storage capacitor (302) which is connected to the source of an MOS transistor (303). The gate of the transistor (303) is controlled by a memory word line (WL), and the source of the transistor is connected to a bit line (BL) as shown in FIG. 2(b). During a memory read operation, one word line (WL) is activated to turn on the transistors (303) in all the memory cells (301) connected to the word line. For the example in FIG. 2(a), we assume 288 bits are read from the memory array (310) during a read operation. These data are divided into 4 groups of 72-bit data; each group contains 64 data bits (D[7:0][7:0]) and 8 ECC bits (C[7:0]). The data read from nearby memory cells are sent to different ECC logic circuits (320-323) as shown in FIG. 2(a). Each set of the ECC logic circuits (320-323) is capable of correcting an erroneous data among its 72 input data. Since the data from nearby memory cells are sent to different ECC logic circuits, errors caused by nearby memory cells can be corrected unless more than 5 nearby memory cells are all wrong. FIGS. 2(c,d) are schematic diagrams of one of those 4 sets of ECC logic circuits 320 in FIG. 2(a). The 72 bit inputs to the ECC logic circuit are grouped into 8 sets of data bits D[7:0][7:0], and 8 ECC bits C[7:0]. The ECC logic (320) comprises 8 identical parity circuit blocks (P7-P0). Schematic diagram of the parity circuit is shown in FIG. 2(d). Each parity circuit (P7-P0) comprises 20 exclusive-or gates (330). The parity circuit P[k] takes data D[k][7:0] and ECC bit Ck as inputs, where k is an integer between 0 to 7. It sends four outputs (N11, N23, N33, N41) to the parity circuit on top of it, and receives corresponding outputs (N11B, N23B, N33B, N41B) from the parity circuit below it. It also sends three outputs (N24, N32, N42) to the parity circuit below it, and receives the corresponding outputs (N24T, N32T, N42T) from the parity circuit above it. It also outputs a correction factor Fk to the memory array and to the output correction circuits. Using the schematic diagram in FIG. 2(d), we can determine the logic function of the outputs of the kth parity circuit (P[k]) as

Detailed Description Text (37):
To understand the method to simplify manufacture technology using ECC method, we must understand the limitations of prior art manufacture technologies. To reduce sub-threshold leakage current, the word line transistor (303) for a prior art DRAM cell must be a long channel transistor with high threshold voltage and thick gate oxide. For performance optimization, high speed logic circuits would like to use short channel transistors with low threshold voltage and thin gate oxide. In order to meet those conflicting requirements, we must build both types of transistor on the same IC; the manufacture technology became more complex than a typical logic technology or a typical DRAM technology. FIGS. 4(a-g) illustrate the manufacture procedures for a prior art high performance IC technology that has both high speed transistors for its logic circuits and low leakage transistors for its DRAM memory cells on the same chip. In the following figures, the cross-section diagrams for an n-channel high performance logic transistor are shown in the left hand side, and the cross-section diagrams for an n-channel low leakage memory transistor are shown in the right hand side for comparison. FIG. 4(a) shows such a side-by-side cross section diagram at threshold voltage implantation (Vt implant) procedure. The active areas of transistors are covered by protection oxide layers (401), and the isolation areas are covered by field oxide layers (403). The threshold voltages of the logic transistor is adjusted by ion implantation (405), and positive dopants (407, 409) are implanted into the active areas of both transistors. Since the memory transistor need to have higher threshold voltage

and thicker gate oxide, additional implantation is needed. FIG. 4(b) shows that another ion implantation (415) is done when the area of the logic transistor is covered with photo-resist (411). The dopant density in the memory transistor (409) is therefore different from that of the logic transistor (407). The next procedure is to remove the protection oxide (401) in the memory transistor while the photo-resist still protects the area for logic transistor, as illustrated in FIG. 4(c). The photo-resist is then removed, and a thin layer of high quality gate oxide (411) is grown in the memory transistor area as shown in FIG. 4(d); the protection oxide 443 at the logic transistor also grows slightly thicker at this stage. The thickness of the gate oxide (411) is exaggerated in all the following diagrams because it would not be visible if drawn to scale. The next step is to cover the memory transistor with photo-resist (451) and remove the protection oxide (443) in the logic area as shown in FIG. 4(e). The photo-resist (451) is then removed before a thin layer of high quality gate oxide (461) is grown in the logic transistor area as shown in FIG. 4(f). In the mean time, the gate oxide in the memory area (463) is grown thicker. All the following procedures, including poly silicon deposition, definition of gate area, interlayer insulator deposition, lightly-doped-region definition, source/drain implantation, are all identical in both types of transistor. Those procedures are well-known to the art so that there is no need to describe them in details. The final structure of both types of transistor are shown in FIG. 4(g). There are three major difference between the logic transistor in the left hand side and the memory transistor in the right hand side. The gate oxide (473) of the logic transistor is thinner than the gate oxide (474) of the memory transistor. Typical oxide thickness is 7 nm for the logic transistor, and 12 nm for the memory transistor. The channel region doping (475) of the logic transistor is different from the channel region doping (476) of the memory transistor so that they have different threshold voltages. Typical threshold voltage (Vt) for the n-channel logic transistor is around 0.5 volts, while typical threshold voltage for the memory transistor is around 0.7 volts. The thin gate, low Vt transistor is optimized to build high speed logic circuits. The thick gate, high Vt transistor is optimized for low leakage current; it also can tolerate higher gate voltages. This technology allows us to build DRAM devices and high performance logic circuits in the same chip, but it requires at least two more masking steps and many more manufacture procedures; the manufacture cost is increased significantly while yield degrades dramatically. One prior art solution is to use the thick gate, high Vt transistor for both memory and logic circuits. This approach reduces complexity in manufacture technology, but it degrades logic circuit performance dramatically; such technology is only useful to build low end products.

Detailed Description Text (38):
When the DRAM array is equipped with the above ECC protection mechanism, the memory refresh requirement is improved by many orders of magnitudes; we can use the same transistor for logic circuits and for memory cells without any charge retention problem. Using methods described in our previous patent applications, we no longer need to use high word line voltage. Therefore, we can achieve high performance by using logic transistors everywhere, and simplify the manufacture technology at the same time. The manufacture procedures of an embedded DRAM technology of the present invention is illustrated in FIGS. 5(a-c). At the first step, the procedure for Vt implant illustrated in FIG. 5(a) is identical to that in FIG. 4(a). Both the logic transistor and the memory transistor received the same implantation, and their channel doping (507, 509) are identical. The next step is to remove protection oxide (401) from both areas simultaneously as shown in FIG. 5(b). Thin layers of high quality gate oxide (521, 523) are grown in both types of transistors simultaneously, as shown in FIG. 5(c). The resulting transistor devices are illustrated in FIG. 5(d). The logic transistor and the memory transistor have identical gate oxide layers (543, 544) and identical channel structures (545, 546). Therefore, they can be manufactured simultaneously. The manufacture procedures described in FIGS. 4(a-g) use 2 masking steps, one gate oxidation, one ion implantation, and one etching step more than the procedures described in FIGS. 5(a-d). All of those manufacture procedures in FIG. 5(a-d) are known in the of IC industry. The circuit design methods of the present invention make it possible to use simpler manufacture technology to achieve better performance, better reliability, and better yield at lower cost.

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L13: Entry 11 of 21 File: USPT Jul 20, 1999

DOCUMENT-IDENTIFIER: US 5925144 A
TITLE: Error correction code circuit that performs built-in self test

Detailed Description Text (2):
With reference to FIG. 1, a circuit generally indicated at 10 has a normal mode of operation and a built-in self test mode of operation. Circuit 10 includes a state-defining means 11 such as a latch, flip-flop, or similar structure for producing a selection signal "N/T" having different values for distinguishing between the normal mode and the test mode. Preferably, circuit 10 is a single integrated circuit and includes an input for receiving an externally generated signal for setting and resetting means 11. Circuit 10 includes an encoder 12 having a linear feedback shift register ("LFSR") with a plurality of feedback taps satisfying a typical primitive generator polynomial. During the normal mode of operation, encoder 12 computes a signal sequence that defines redundancy data. Input data D.sub.in are shifted into encoder 12 and the redundancy data are shifted out of encoder 12. The redundancy data are appended to the input data D.sub.in, thus forming a codeword in accordance with a particular code, preferably a Reed-Solomon code. Encoder 12 suitably has the structure of the type of encoder used in a host interface and disk controller integrated circuit which receives user data from a host and responds thereto to generate redundancy data in the form of error correction code check bytes. Such a disk controller is disclosed in the above-identified Incorporated ECC Disclosure.

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L13: Entry 14 of 21 File: USPT Jun 18, 1996

DOCUMENT-IDENTIFIER: US 5528607 A
TITLE: Method and apparatus for protecting data from mis-synchronization errors

Brief Summary Text (19):
Specifically, the encoder encodes the data symbols in accordance with an ECC over GF(2.sup.m), and produces k m-bit ECC symbols. The encoder includes, for encoding the constant, an m-stage linear feedback shift register (LFSR), which is set-up in accordance with a maximum length polynomial in GF(2). The LFSR is pre-set, or hardwired, to initialize to the selected initial coset leader constant. In the preferred embodiment the coset leader is encoded over GF(2), the initial coset leader constant is 100001011, and the encoder is set-up in accordance with the polynomial X.sup.9 +X.sup.8 +X.sup.7 +X.sup.3 +X.sup.2 +1.

Brief Summary Text (20):
To produce the ECC symbols, the encoder encodes the data symbols in a conventional manner using an ECC-symbol generator and produces, in k 9-bit registers, the k ECC symbols. When the first of the ECC symbols is shifted out of the generator, the LFSR is initialized, so that it contains the initial coset leader constant. The contents of the LFSR are then XOR'd with the first ECC symbol.

Brief Summary Text (21):
The LFSR is then shifted to update its contents in accordance with the polynomial set forth above. This produces in the stages of the LFSR a next coset leader constant, which is XOR'd with the next ECC symbol shifted out of the ECC symbol generator. This shifting and XOR'ing continues until each of the ECC symbols produced by the ECC-symbol generator has been combined with a corresponding coset leader constant produced in the LFSR.

Brief Summary Text (23):
The corresponding decoder uses the same LFSR to produce the coset leader constants that are removed from a retrieved code word. The decoder also includes a demodulator, which demodulates retrieved information into code word symbols. As the demodulator shifts out the ECC symbols, the decoder XOR's them with the contents of the LFSR, shifting the LFSR to generate a succession of coset leader constants, as discussed above.

Brief Summary Text (24):
The hardware required to produce the coset/leader is minimized by using the hardwired LFSR. Accordingly, a k-symbol buffer is not needed. Further, there is no delay introduced into the encoding or decoding operations by the LFSR, since the LFSR supplies the coset leader constants to the XOR gate at the same times as the encoder or decoder supplies to the gate the corresponding ECC symbols.

Detailed Description Text (9):
When the first ECC symbol is shifted out of the generator 12 to the XOR circuit 16, the LFSR 40 is at the same time re-set to contain the initial coset leader constant. The contents of the k stages of the LFSR are then combined by XOR circuit 16 with the corresponding m bits of the first ECC symbol. The XOR circuit 16 preferably consists of m 2-bit XOR gates (not shown), which operate in parallel.

Detailed Description Text (10):
As the next ECC symbol is shifted out of the ECC generator 12, the LFSR 40 is also shifted and its contents again applied to XOR circuit 16, this time as the second coset leader constant. The XOR circuit 16 XOR's the constant and the ECC symbol, and produces a next symbol for recording. The two generators and the XOR circuit continue producing the various symbols and constants until all k of the ECC symbols have been combined with the corresponding coset leader constants.

Detailed Description Text (11):
In an alternative embodiment, the coset leader generator may be shifted a total of k times and the initial coset leader constant used only to initialize the LFSR, rather than as the first symbol of the coset leader. The LFSR is thus re-set before the first ECC symbol is shifted out of the generator and thereafter shifted each time the ECC symbol generator is shifted.

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L13: Entry 18 of 21 File: USPT Oct 8, 1991

DOCUMENT-IDENTIFIER: US 5056089 A
**** See image for Certificate of Correction ****
TITLE: Memory device

Detailed Description Text (7):
In the case of an E.sup.2 PROM having a page-mode writing function, the ECC code register 60 may be constituted by, for example, a linear feedback shift register (LFSR). In such an arrangement, the ECC code 30e generated by the ECC code generating circuit 30 on the basis of a plurality of write data 20d is converted into compressed data in accordance with a control clock supplied from a microprocessor, and is then stored in the LFSR. After all of a plurality of test patterns have been input, the contents of the LSFR are read out and compared with an expected value, so that it is possible to immediately check a single function of the ECC code generating circuit 30.

CLAIMS:

4. The memory system according to claim 2 wherein said register is a linear feedback shift register (LFSR) for controlling said memory device to sequentially input a plurality of test patterns to said ECC code generating circuit, to compress the ECC code output from said ECC code generating circuit in accordance with the test patterns, and to check said ECC code generating circuit on the basis of the result.

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L27: Entry 3 of 14 File: USPT Jul 23, 2002

DOCUMENT-IDENTIFIER: US 6424926 B1
TITLE: Bus signature analyzer and behavioral functional test method

Brief Summary Text (7):
Subsequently, structural testing methods and systems were developed called built-in self-test (BIST) to test the individual internal integrated circuits of the equipments. Examples of these methods include a Linear Feedback Shift Register (LFSR) and a Multiple Input Signature Registers (MISR), which is a variant of the LFSR. Both the LFSR and MISR are used to perform signature analysis of the chip being tested. An example of one of many possible configurations of a generic MISR 200, which can be used as a signature analyzer, is shown in FIG. 2. In FIG. 2, the generic MISR 200 is illustrated in which n-bit D-type flip-flops 210-1-210-n are serially coupled together and coupled to a feedback circuit 220 to produce compressed signatures on every clock cycle. While the feedback circuit is shown feeding back an output signal Q from the nth flip-flop of the serially-connected flip-flops 210-1-210-n to each flip-flop 210-1-210-n, the feedback circuit can be configured to feedback to any number of the flip-flops 210-1-210-n. However, since the generic MISR 200 compresses the signal on every clock cycle, regardless of whether it is a valid bus cycle or not, the generic MISR 200 is vulnerable to X-states and circuit glitches. "X-states" are unknown and undefined processor states which can occur during processor execution of application programs as a result of, for example, uninitiated nodes, signal contention as a result of internal circuit conflicts, and/or circuit glitches. "Circuit glitches" can include, for example, errors, transients and/or unintelligible signals.

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L27: Entry 11 of 14 File: USPT Jan 17, 1995

DOCUMENT-IDENTIFIER: US 5383143 A
TITLE: Self re-seeding linear feedback shift register (LFSR) data processing system for generating a pseudo-random test bit stream and method of operation

Detailed Description Text (61):
Other modifications that are possible are: the addition of an OR or NOR gate to the PRPG LFSR that combines all of the Q-outputs into a single signal that can be used to detect the error state of all 0's; the usage of different configurations of signature analyzers (multiple parallel inputs with feedback from the end only, multiple parallel inputs with feedback distributed through the middle stages, single serial input with feedback from the end only, and single serial input with feedback distributed through the middle states) that can be any bit length; esoteric multiples of the PRPG LFSR control circuit such as two or more PRPG LFSRs with different initial seeds supplying multiple scan chains; and the ability to run the entire test more than once by including the ability to match the initial state more than two times (adding a count stage for the final enable or done signal that requires returning to the initial seed more than some cutoff value). It is to be understood, therefore, that this invention is not limited to the particular forms illustrated and that it is intended in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention.

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L36	L34 same lfsr	22	L36
L35	L34 and lynch	3	L35
L34	L28 same configur$	44	L34
L33	L31 same bist	37	L33
L32	L31 and l22	0	L32
L31	L4 same memory	43	L31
L30	L29 same ecc	25	L30
L29	L28 or l12	768	L29
L28	misr	163	L28
L27	L14 same error	14	L27
L26	L23 and l4	0	L26
L25	L23 and l14	1	L25
L24	L23 and l13	0	L24
L23	L22 same memory	3518	L23
L22	L21 or l19 or l20	22875	L22
L21	multilevel	9355	L21
L20	multi-level	10780	L20
L19	multiple adj1 level	6440	L19
L18	L15 same l12	0	L18
L17	L15 and l14	0	L17
L16	L15 same l14	0	L16
L15	multilevel same memory	1327	L15
L14	L12 same configur$	181	L14
L13	L12 same l2	21	L13
L12	lfsr	689	L12
L11	L10 same circuit	66	L11
L10	L2 same l6	197	L10
L9	L8 same l6	2	L9
L8	error-check	137	L8
L7	L1 same l2 same l6	1	L7
L6	interconnect$	448752	L6
L5	l1 same l2 same l3	4	L5
L4	bisr	59	L4
L3	identical	670927	L3
L2	ecc	6424	L2
L1	logic adj1 circuit	61026	L1

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L33: Entry 6 of 37 File: USPT Oct 8, 2002

DOCUMENT-IDENTIFIER: US 6462995 B2
TITLE: Semiconductor memory device capable of recovering defective bit and a system having the same semiconductor memory device

Brief Summary Text (22):
FIG. 6 shows a flowchart of test procedure of the memory by the BISR. In the final die sort by the function test, first, memory test by the BIST is carried out (step S1a). If a defect is detected (YES in step S1b), if the defect may be recovered (YES at step S1c), the defective bit is replaced with redundant column (step S1d). Then, the function test is carried out (step S1e). and the defective bit is checked again (step S1f), so as to determine whether or not the object memory is acceptable. In the memory test using the BIST, the fuse melting-down step (step S2) and post-test test processing (step S16) are still necessary.

Detailed Description Text (27):
First, the redundancy information (fault information) of the defective bit extracted by the BIST of the volatile semiconductor memory device is stored in the register 116 of the BISR circuit 15.

Detailed Description Text (42):
The semiconductor memory device according to the fourth embodiment is provided with a control voltage source 21 in addition to the structure shown in FIG. 4 as compared to the structure of the above described BIST/BISR.

Detailed Description Text (44):
The control voltage source 21 is controlled by a test controller 22 of the BIST/BISR (built-in self-repair) circuit 11b, and an output voltage turns to an access voltage for a memory cell. Recently, many semiconductor memory devices use plural different power supply voltages. Such a semiconductor memory device is provided with a limiter circuit for controlling a charge pump or an output voltage of this charge pump to generate plural different voltages. By adjusting the limiter circuit, the access voltage for checking the aforementioned operating margin can be generated with the charge pump easily.

Detailed Description Text (45):
FIG. 12 shows an exemplary test flowchart of the BIST/BISR of the fourth embodiment. First, the test controller 22 sets the access voltage to a nominal voltage, generates various test patterns and expected values, sends them to the memory block and determines whether or not each of them is acceptable (step S121). Likewise, the test is carried out at a voltage higher than the nominal voltage by about 10% and a voltage lower by 10%, for example, so as to screen memory cells having a small operating margin (steps S122, S123). If a sufficiently large margin is secured with a high voltage or a low voltage, a margin against a change in temperature due to, for example, continuous operation can be secured.

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L33: Entry 14 of 37 File: USPT Nov 27, 2001

DOCUMENT-IDENTIFIER: US 6324106 B1
TITLE: Semiconductor memory device capable of recovering defective bit and a system having the same semiconductor memory device

Brief Summary Text (18):
FIG. 6 shows a flowchart of test procedure of the memory by the BISR. In the final die sort by the function test, first, memory test by the BIST is carried out (step S1a). If a defect is detected (YES in step S1b), if the defect may be recovered (YES at step S1c), the defective bit is replaced with redundant column (step S1d). Then, the function test is carried out (step S1e) and the defective bit is checked again (step S1f), so as to determine whether or not the object memory is acceptable. In the memory test using the BIST, the fuse melting-down step (step S2) and post-test test processing (step S16) are still necessary.

Detailed Description Text (27):
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The semiconductor memory device according to the fourth embodiment is provided with a control voltage source 21 in addition to the structure shown in FIG. 4 as compared to the structure of the above described BIST/BISR.

Detailed Description Text (44):
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Detailed Description Text (45):
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L35: Entry 1 of 3 File: USPT Jul 23, 2002

DOCUMENT-IDENTIFIER: US 6424926 B1
TITLE: Bus signature analyzer and behavioral functional test method

Brief Summary Text (7):
Subsequently, structural testing methods and systems were developed called built-in self-test (BIST) to test the individual internal integrated circuits of the equipments. Examples of these methods include a Linear Feedback Shift Register (LFSR) and a Multiple Input Signature Registers (MISR), which is a variant of the LFSR. Both the LFSR and MISR are used to perform signature analysis of the chip being tested. An example of one of many possible configurations of a generic MISR 200, which can be used as a signature analyzer, is shown in FIG. 2. In FIG. 2, the generic MISR 200 is illustrated in which n-bit D-type flip-flops 210-1-210-n are serially coupled together and coupled to a feedback circuit 220 to produce compressed signatures on every clock cycle. While the feedback circuit is shown feeding back an output signal Q from the nth flip-flop of the serially-connected flip-flops 210-1-210-n to each flip-flop 210-1-210-n, the feedback circuit can be configured to feedback to any number of the flip-flops 210-1-210-n. However, since the generic MISR 200 compresses the signal on every clock cycle, regardless of whether it is a valid bus cycle or not, the generic MISR 200 is vulnerable to X-states and circuit glitches. "X-states" are unknown and undefined processor states which can occur during processor execution of application programs as a result of, for example, uninitiated nodes, signal contention as a result of internal circuit conflicts, and/or circuit glitches. "Circuit glitches" can include, for example, errors, transients and/or unintelligible signals.

US Reference Patentee Name (2):
Lynch

US Reference Group (2):
4608691 19860800 Lynch 714/732

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